What is claimed is:

1. A semiconductor integrated circuit device provided with a memory macro for conducting access operation to a plurality of memory cells arranged in memory cell array under normal operation by selecting a logical row region and a logical column region that are in a basic region within a logical address space of the memory cell array, the semiconductor integrated circuit device comprising:

a defective region detecting section for detecting whether or not a defective memory cell exits by each physical row region or each physical column region based on physical layout of the memory cell array;

at least one unit of redundancy region for remedying a defective memory cell by each physical row region or each physical column region in accordance with a detection result obtained by the defective region detecting section;

an allocating section for allocating at least one unit of the physical row region or the physical column region to one unit of the logical row region or the logical column region, respectively.

2. A semiconductor integrated circuit device according to claim 1, wherein the physical row region or the physical column region is a minimum unit electrically controllable in view of physical layout of the memory cell array.

3. A semiconductor integrated circuit device according to claim 1, wherein

the physical row region is a plurality of the memory cells to be selected by at least one word line electrically and

individually controllable out of a plurality of word lines physically arranged in the memory cell array, and

the physical column line is a plurality of the memory cells to be selected by at least one bit line electrically and individually controllable out of a plurality of bit lines physically arranged in the memory cell array.

4. A semiconductor integrated circuit device provided with a memory macro and a logical macro and operable along with a clock signal supplied from an external section, the semiconductor integrated circuit device comprising:

a self-test circuit for conducting a test of the memory macro, the self-test circuit being operable apart from the logical macro and; and

a frequency controlling section for converting the clock signal into an internal clock signal that is a maximum frequency of the memory macro when the test of the memory macro is conducted.

5. A semiconductor integrated circuit device according to claim 4, wherein the frequency controlling section converts the clock signal based on test condition information supplied from an external section.

6. A semiconductor integrated circuit device according to claim 5, wherein the test condition information relates to information on division/multiplication of the clock signal.

7. A semiconductor integrated circuit device according to claim 4, wherein the memory macro includes two or more of memory cell

array maximum frequency of which differ from each other, and the frequency controlling section outputs the internal clock signal suitable to the memory cell array subject to the test.

8. A semiconductor integrated circuit device according to claim 7 further comprising a clock-supply switching section for supplying the internal clock signal to corresponding memory cell array.

9. A semiconductor integrated circuit device provided with a memory macro with self-test function for memory cell array, the semiconductor integrated circuit device comprising:

a data-latency controlling section for controlling latency of data inputted/outputted from the memory cell array;

a set-latency-value switching section for supplying a first-latency-value information to be set in normal operation and a second-latency-value information to be set in self-test; and

a latency-value storing section for storing the second-latency-value information.

10. A semiconductor integrated circuit device according to claim 9, wherein

the first-latency-value information is information of a latency value needed for operating the memory macro as a function circuit, and

the second-latency-value information is information of a latency value needed for operation by maximum frequency of the memory macro.

11. A semiconductor integrated circuit device according to claim

9, wherein the second-latency-value information is stored in the latency-value storing section based on test condition information supplied from an external section.

12. A semiconductor integrated circuit device according to claim 11, wherein the test condition information is information relating to the second-latency-value information.

13. A semiconductor integrated circuit device according to claim 9, wherein the memory macro includes two or more of memory cell array second-latency-value information of which differ from each other, and the latency-value storing section outputs the second-latency-value information suitable to the memory cell array subject to the test.

14. A semiconductor integrated circuit device according to claim 13 further comprising a latency-value-supply switching section for supplying the second-latency-value information stored in the latency-value storing section to corresponding memory cell array.

15. A semiconductor integrated circuit device provided with a memory macro with self-test function for memory cell array, the semiconductor integrated circuit device comprising:

a defective region storing section for storing a detection result indicating presence/absence of a defective memory cell for each of predetermined regions in the memory cell array; and

an output latency controlling section for controlling output latency of the detection result depending on propagation delay time to propagate from the defective region storing section through an output path and operation frequency of the clock

signal when the detection result is outputted based on a clock signal supplied from an external section.

16. A semiconductor integrated circuit device according to claim 15, wherein, in the output latency controlling section, an output latency value is adjusted based on test condition information supplied from an external section.

17. A semiconductor integrated circuit device according to claim 16, wherein the test condition information relates to the output-latency-value information.

18. A self-test method of memory macro built in a semiconductor integrated circuit device that includes a memory macro for conducting access operation to a plurality of memory cells arranged in memory cell array under normal operation by selecting a logical row region and a logical column region that are in a basic region within a logical address space of the memory cell array, the self-test method comprising steps of:

test-unit extracting step where the logical row region or the logical column region is divided out to at least one unit of physical row region or physical column region, respectively, based on physical layout of the memory cell array; and

defective-region extracting step where absence/presence of a defective memory cell is detected for each physical row region or each physical column region.

19. A self-test method of memory macro built in a semiconductor integrated circuit device that includes a memory macro and a logical macro and is operable along with a clock signal supplied

from an external section, the self-test method comprising steps of:

control stopping step where control of the memory macro by the logical macro is stopped based on a self-test-start command; and

test-clock supplying step where the clock signal is converted with reference to the memory macro so that an internal clock signal equivalent to operable frequency of the memory macro is supplied by a self-test-start command.

20. A self-test method of memory macro built in a semiconductor integrated circuit device provided with a memory macro for conducting data-input/data-output from memory cell array, the self-test method comprising steps of:

test-latency-value storing step where test-latency-value information with reference to data inputted/outputted from the memory cell array is stored when self test is conducted;

test-latency-value setting step where the test-latency-value information is set in accordance with a self-test-start command; and

a data-latency controlling step where latency of data inputted/outputted from the memory cell array is controlled in accordance with the test-latency-value information set in the test-latency value setting step.

21. A self-test method of memory macro built in a semiconductor integrated circuit device provided with a memory macro for conducting data-input/data-output from memory cell array, the self-test method comprising steps of:

defective-region storing step where a detection result of

presence/absence of a defective memory cell is stored for each of predetermined regions within the memory cell array;

output-latency determining step where an output latency value of the detection result is determined based on propagation delay time until an output of the detection result and operation frequency of the clock signal when the detection result is to be outputted based on a clock signal supplied from an external section; and

defective-region outputting step where the detection result is outputted in form of the output latency value based on the clock signal.